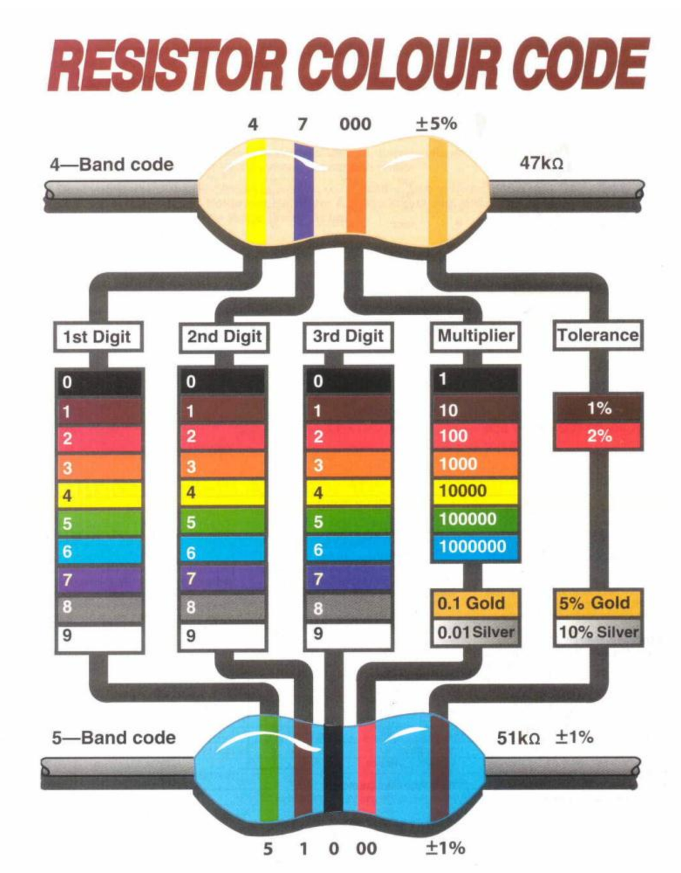
REFERENCE SHEET

Multiplication Factor	Prefix Name	Prefix Symbol
$1\ 000\ 000\ 000\ 000 = 10^{12}$	tera	T
$1\ 000\ 000\ 000 = 10^{9}$	giga	G
$1\ 000\ 000 = 10^{6}$	mega	M
$1\ 000 = 10^{3}$	kilo	k
$100 = 10^{2}$	hecto	h
$10 = 10^{1}$	deka	da
$0.1 = 10^{-1}$	deci	d
$0.01 = 10^{-2}$	centi	c
$0.001 = 10^{-3}$	milli	m
$0.000\ 001 = 10^{-6}$	micro	μ
$0.000\ 000\ 001 = 10^{-9}$	nano	n
$0.000\ 000\ 000\ 001 = 10^{-12}$	pico	p

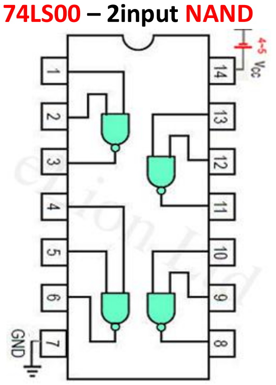
This table shows the common prefixes. Others, from 10^{-24} to 10^{24} are acceptable for use of the SI. See NIST SP 330.



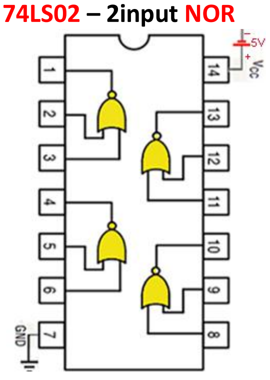
Quantity	Symbol	Unit
Current	I	Ampere (A)
Voltage	V	Volt (V)
Resistance	R	Ohm (Ω)
Frequency	f	Hertz (Hz)
Capacitance	C	Farad (F)
Inductance	L	Henry (H)
Power	P	Watt (W)

INTEGRATED CIRCUIT DATA SHEETS

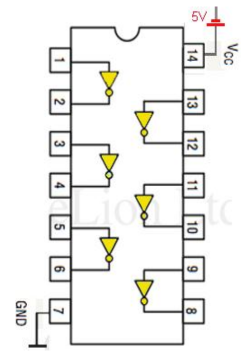
74LS00 – 2input NAND



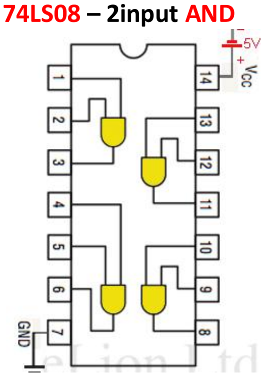
74LS02 – 2input NOR



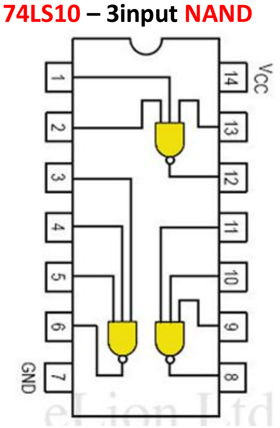
74LS04 - INVERTER



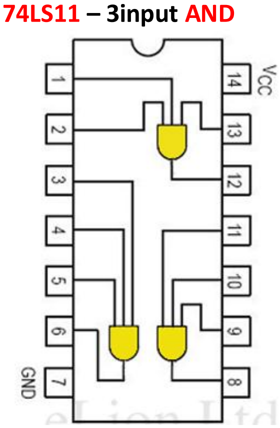
74LS08 – 2input AND



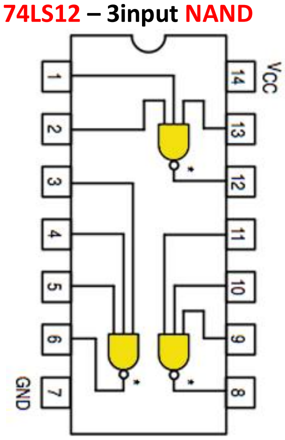
74LS10 – 3input NAND



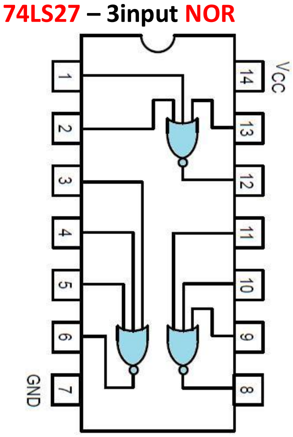
74LS11 – 3input AND



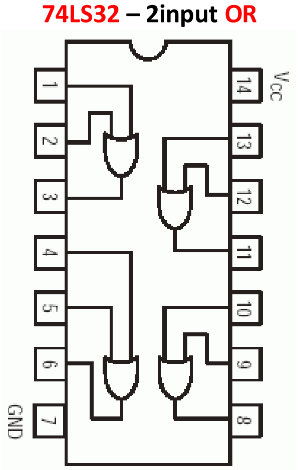
74LS12 – 3input NAND



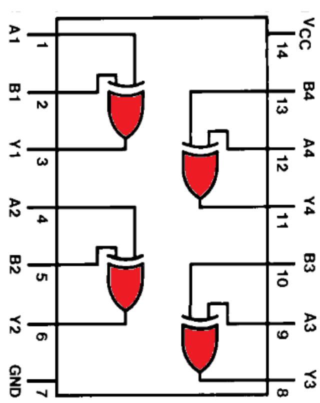
74LS27 – 3input NOR



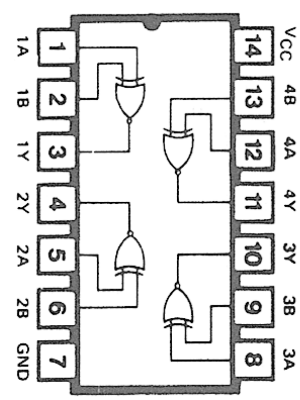
74LS32 – 2input OR



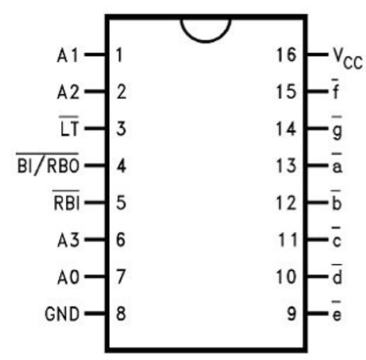
74LS86 – 2input XOR



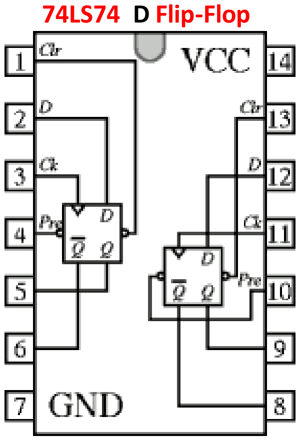
74LS266 – 2input XNOR



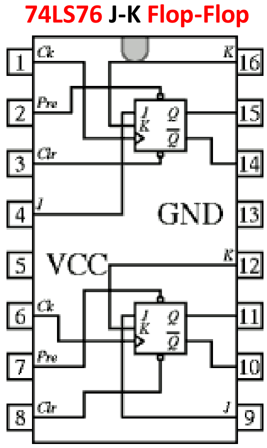
74LS47 – 7 Display Driver



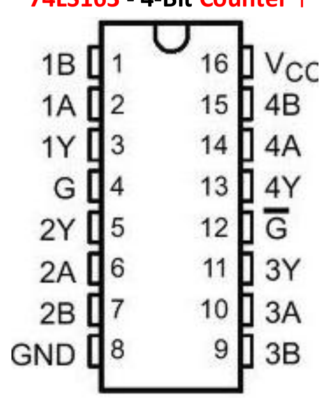
74LS74 D Flip-Flop



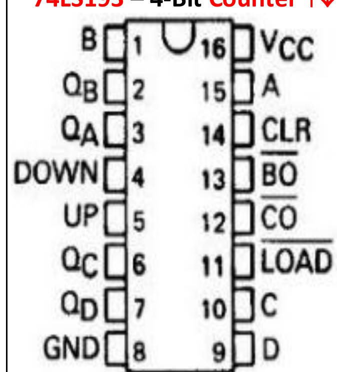
74LS76 J-K Flop-Flop



74LS163 - 4-Bit Counter ↑



74LS193 – 4-Bit Counter ↑↓

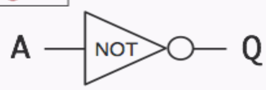


NOT	
A	Q
0	1
1	0

$Q = \neg A$

also written

$Q = \overline{A}$



AND		
A	B	Q
0	0	0
0	1	0
1	0	0
1	1	1

$Q = A \cap B$

also written

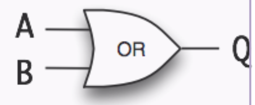
$Q = A \bullet B$

OR		
A	B	Q
0	0	0
0	1	1
1	0	1
1	1	1

$Q = A \cup B$

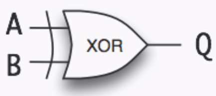
also written

$Q = A + B$



XOR		
A	B	Q
0	0	0
0	1	1
1	0	1
1	1	0

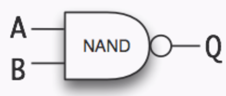
$Q = A \oplus B$



$A\overline{B} + \overline{A}B = A \oplus B$

NAND		
A	B	Q
0	0	1
0	1	1
1	0	1
1	1	0

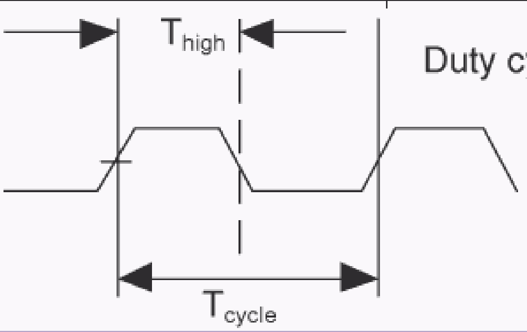
$Q = \neg(A \cap B)$



XNOR		
A	B	Q
0	0	1
0	1	0
1	0	0
1	1	1

$Q = \overline{A \oplus B}$

$\overline{A \oplus B}$

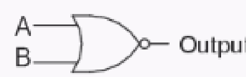


$$\text{Duty cycle} = \frac{T_{high}}{T_{cycle}}$$

NOR

$Z = \overline{OR}$

A	B	Output
0	0	1
0	1	0
1	0	0
1	1	0



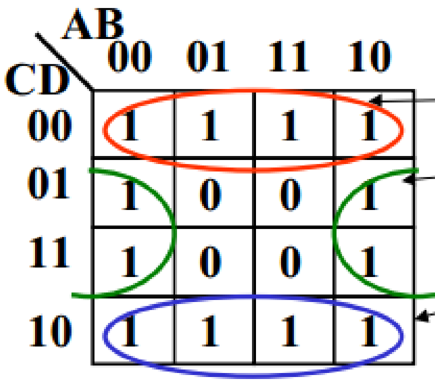
Boolean Algebra Laws

OR	AND
1 + 0 = 1	1 · 0 = 0
0 + 1 = 1	0 · 1 = 0
0 + 0 = 0	0 · 0 = 0
1 + 1 = 1	1 · 1 = 1

Multiplicative	Additive
A · 0 = 0	A + 0 = A
A · 1 = A	A + 1 = 1
A · A = A	A + A = A
$A \cdot \overline{A} = 0$	$A + \overline{A} = 1$

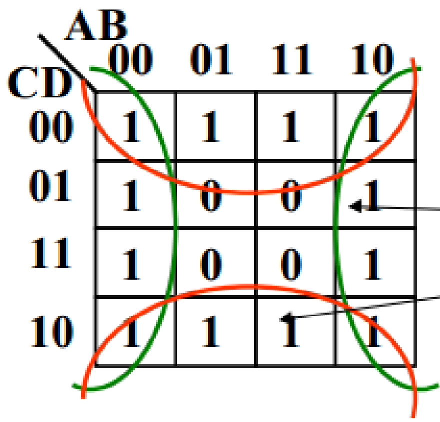
Commutative Law	A·B = B·A	A+B = B+A
Associative Law	(AB)C = A(BC)	(A+B)+C = A+(B+C)
Distributive Law	A(B+C) = AB+AC	(A+B)(A+C)=A+BC
Absorption Law (Consensus Theorem)	A+AB = A + B $\overline{A}+AB = \overline{A}+B$ $A+\overline{A}\,\overline{B} = A+\overline{B}$ $\overline{A}+A\overline{B} = \overline{A}+\overline{B}$	A + AB = A $AB + A\overline{B} = A$ A(A+B) = A $(A+\overline{B})B = AB$
Double Complement	$\overline{\overline{A}} = A$	
DeMorgan's Law	$\overline{AB} = \overline{A}+\overline{B}$	$\overline{A+B} = \overline{A}\,\overline{B}$

K MAPPING

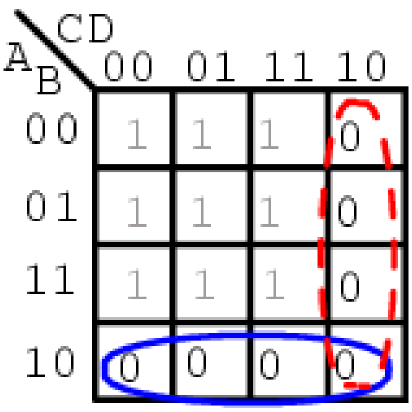


F (A,B,C,D) = B'D + C'D' + CD'

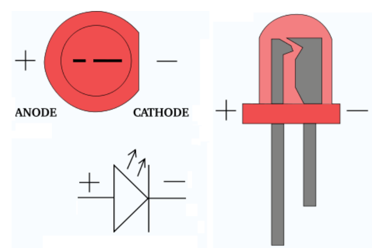
Want LARGEST groupings that can cover '1's.



F (A,B,C,D) = B' + D'

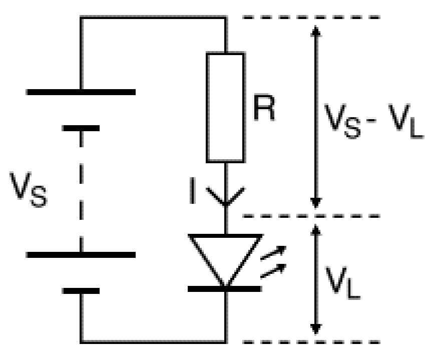


$$F = (\overline{A} + B)(\overline{C} + D)$$



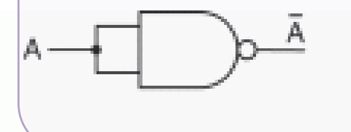
An LED must have a resistor connected in series to limit the current through the LED, otherwise it will burn out almost instantly.

$$R = (V_S - V_L) / I$$

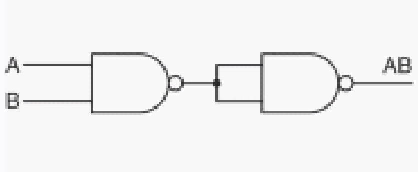


NAND SUBSTITUTION

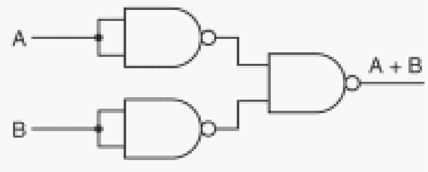
INVERTER



AND

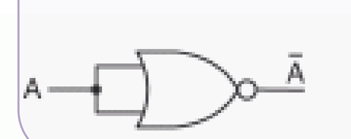


OR

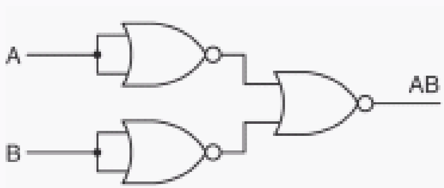


NOR SUBSTITUTION

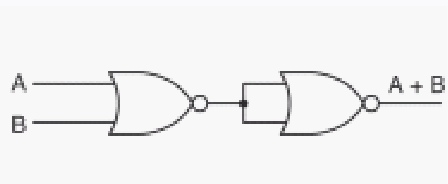
INVERTER



AND

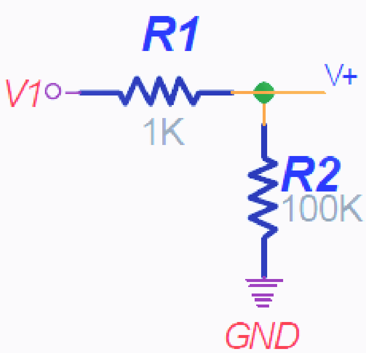


OR

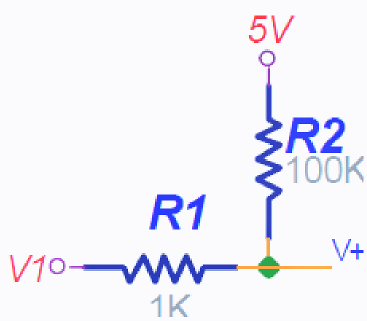


VOLTAGE DIVIDER

Pull Down

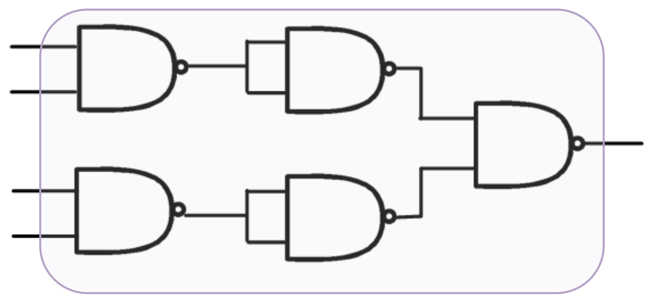


Pull Up



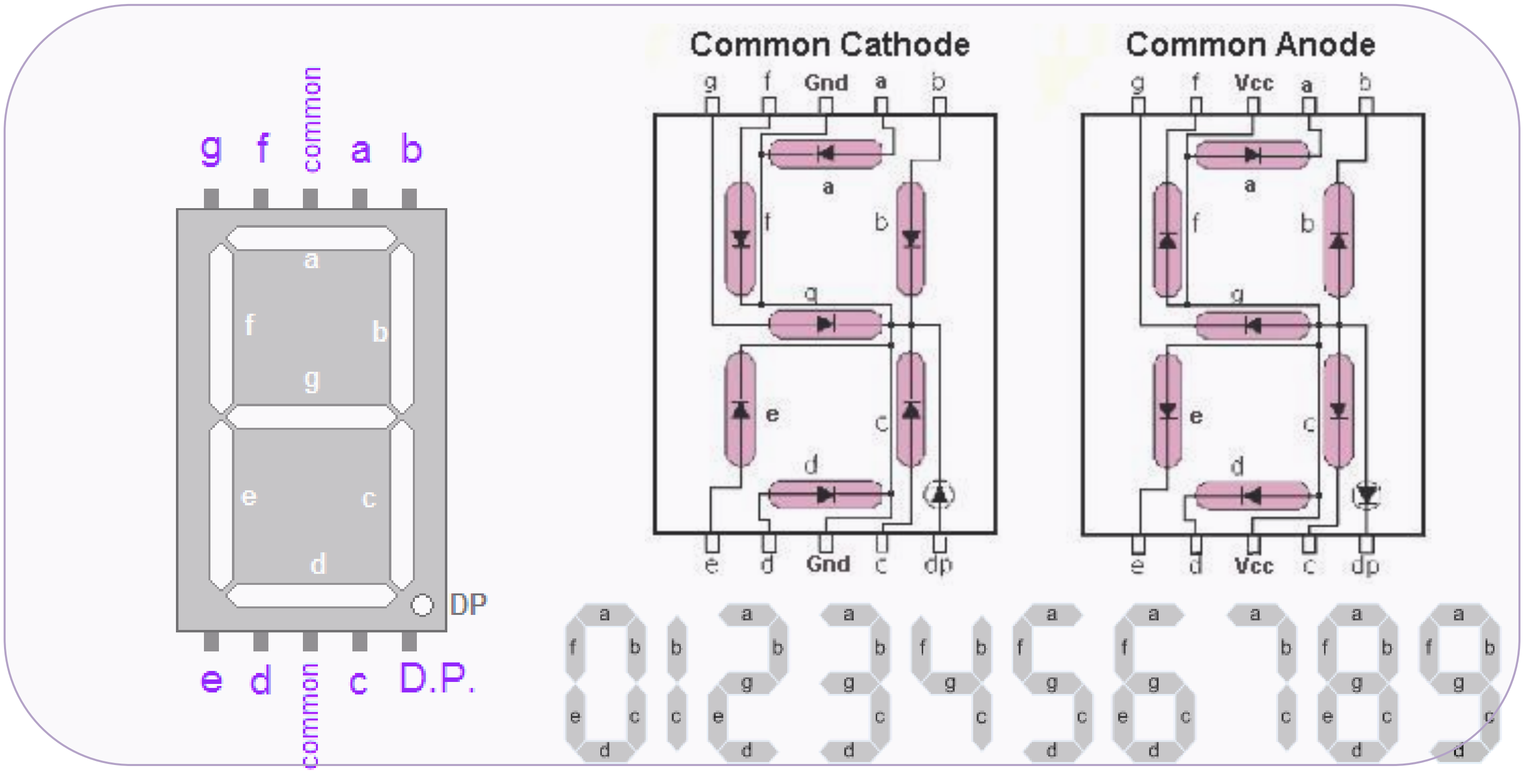
$$\frac{V_{out}}{V_{in}} = \frac{IR_2}{I(R_1 + R_2)} = \frac{R_2}{R_1 + R_2}$$

4-input NAND using 2-input NANDs



Seven Segment LED

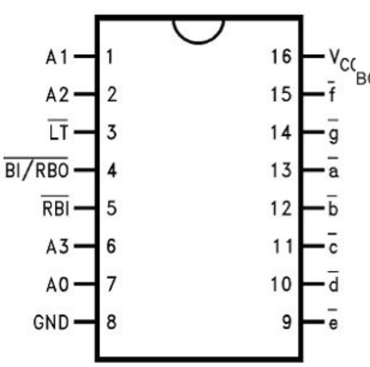
Seven segment displays come in two varieties - Common Anode (CA) and Common Cathode (CC).
CA is illuminated by LOW voltage (less than 0.7V). CC is illuminated by HIGH voltage. (greater than 0.7V)

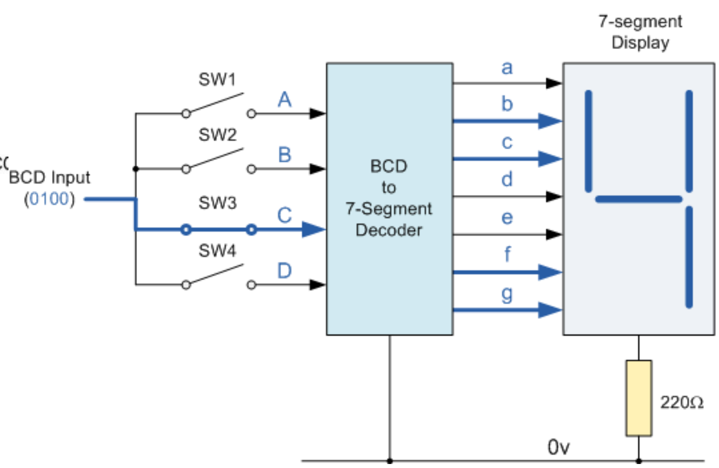


7-Segment Display Decoders/Drivers

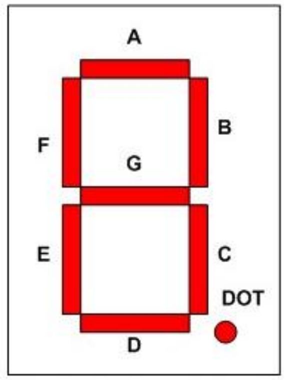
(74LS47-Common Anode *or* 74LS48-Common Cathode)

74LS47

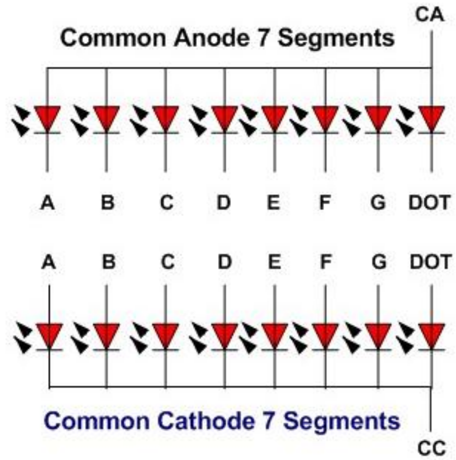




Typical 7 Segments Display



The 7 Segment's Name and the DOT



The Seven Segments Display

Common Anode Display Table

BCD inputs				segment outputs							display
D	C	B	A	a	b	c	d	e	f	g	
0	0	0	0	1	1	1	1	1	1	0	0
0	0	0	1	0	1	1	0	0	0	0	1
0	0	1	0	1	1	0	1	1	0	1	2
0	0	1	1	1	1	1	1	0	0	1	3
0	1	0	0	0	1	1	0	0	1	1	4
0	1	0	1	1	0	1	1	0	1	1	5
0	1	1	0	0	0	1	1	1	1	1	6
0	1	1	1	1	1	1	0	0	0	0	7
1	0	0	0	1	1	1	1	1	1	1	8
1	0	0	1	1	1	1	0	0	1	1	9

F L I P – F L O P S and L A T C H E S

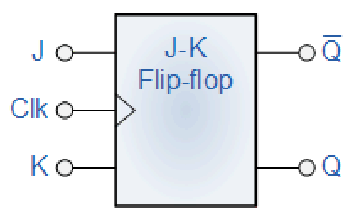
JK FLIP-FLOP (74LS76)

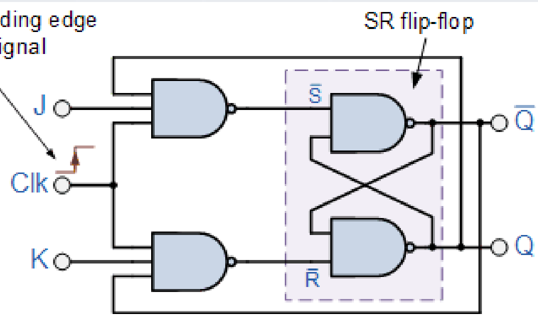
	J	K	Q	Q̅	Description
↑	0	0	1	0	Memory no change
	0	0	0	1	
	0	1			Reset Q » 0
	0	1			
	1	0			Set Q » 1
	1	0			
toggle action	1	1	0	1	Toggle
	1	1	1	0	

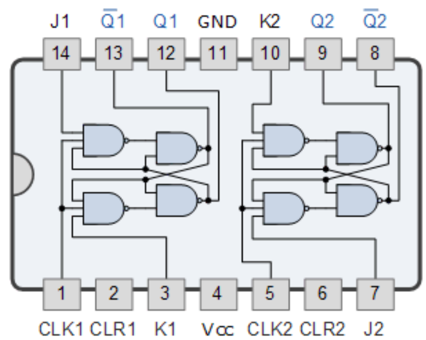
J≠K:
J=1 ⇒ Q=1
J=0 ⇒ Q=0

J=K=0:
Nothing changes

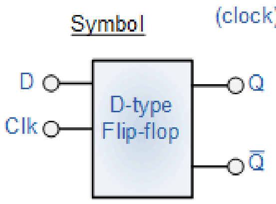
J=K=1:
Toggle/Complement/Both change

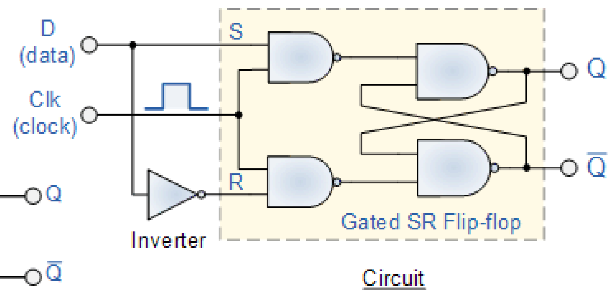




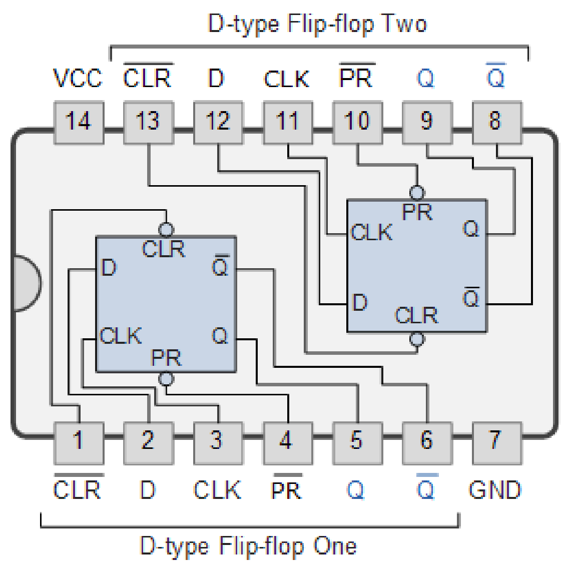


Data FLIP-FLOP (74LS74)



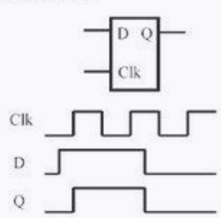


Clk	D	Q	Q̅	Description
↓ » 0	X	Q	Q̅	Memory no change
↑ » 1	0	0	1	Reset Q » 0
↑ » 1	1	1	0	Set Q » 1

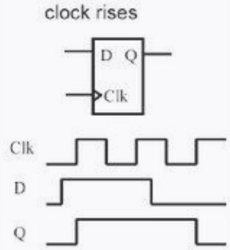


flip flop vs latch:

- Latch
  stores data when clock is low

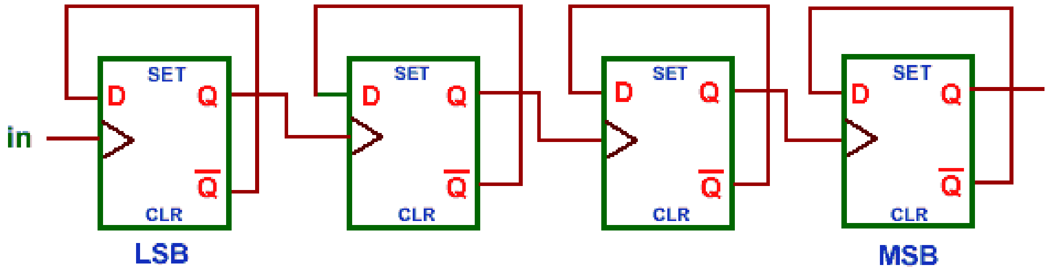


- Flip-Flop
  stores data when clock rises



ASYNCHRONOUS RIPPLE COUNTERS

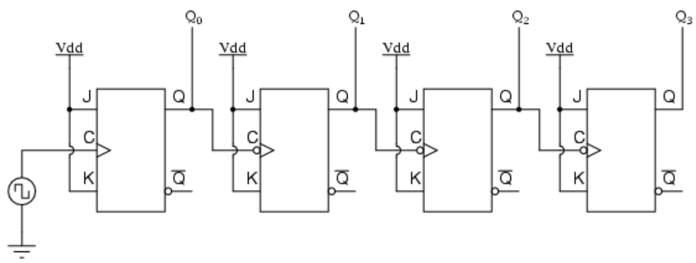
(each divides by two)

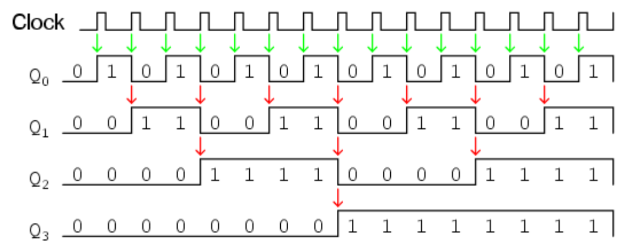


ASYNCHRONOUS COUNTER

(each stage divides by two)

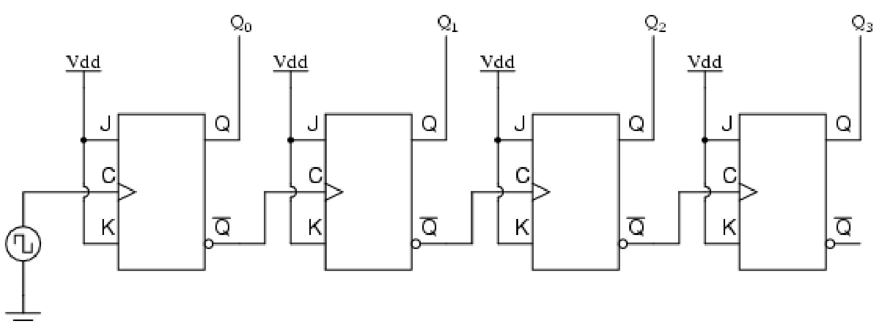
A four-bit "up" counter



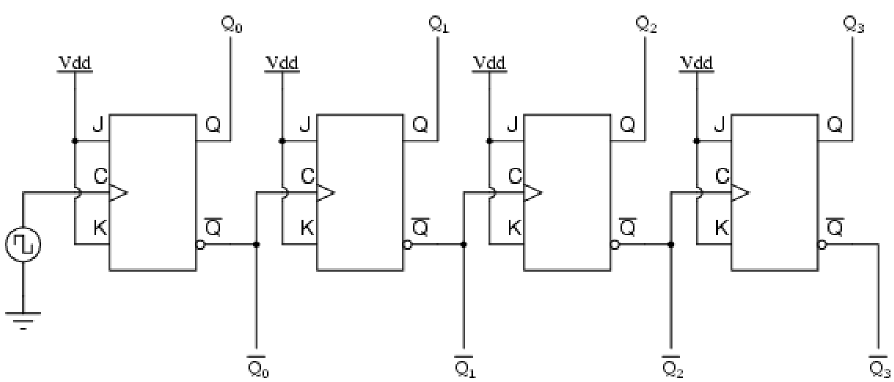


A different way of making a four-bit "up" counter

4 Bit, Binary Ripple Counter



A simultaneous "up" and "down" counter

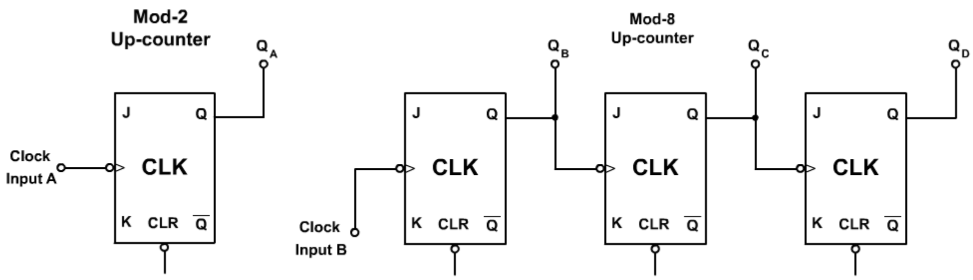


74LS93 4-Bit Asynchronous counter

The 7493 IC is an up-counter that is capable of operating as a multi-modulus counter.

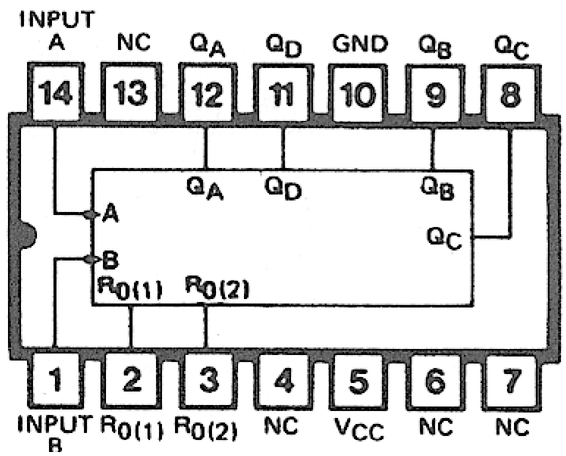
It is constructed of two negative-edge triggered counters that in their natural state are:

- A mod-2 up-counter
- A mod-8 up-counter



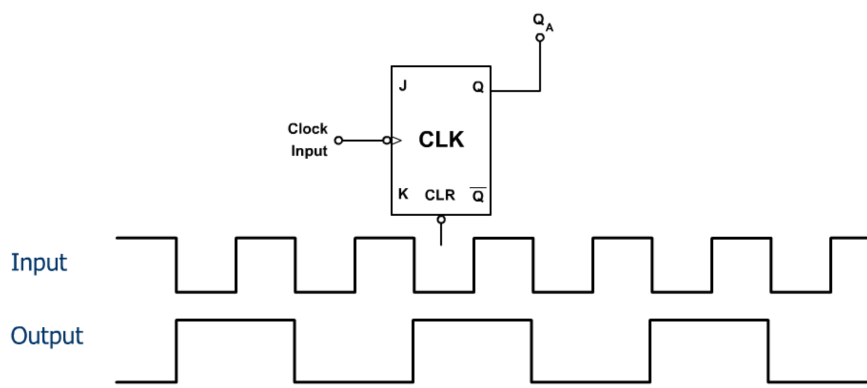
74LS93

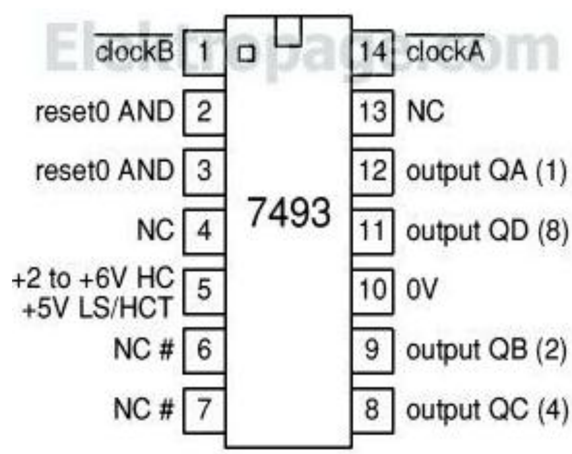
4-bit Binary Counter IC



The Mod-2 Counter

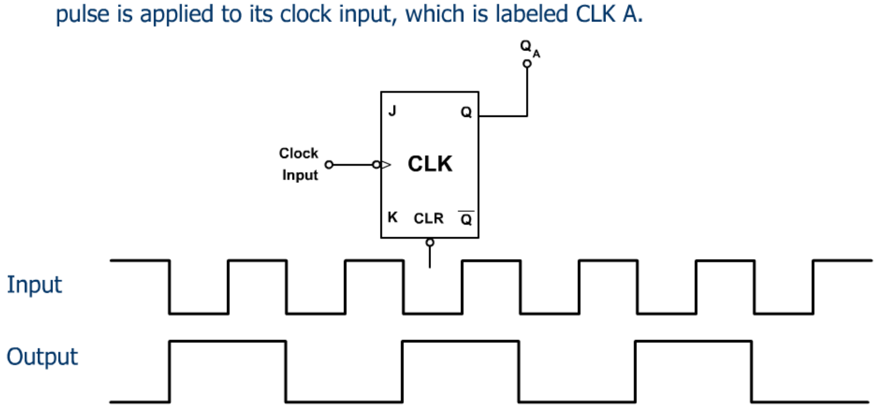
- Used by itself, Flip-flop A operates as a mod-2 counter.
- The count begins with a 0 at the Q output, and the maximum count occurs when the Q output is at a 1.
- The counter recycles back to 0 when the next clock pulse is applied.
- The mod-2 counter changes its count every time a negative edge of a clock pulse is applied to its clock input, which is labeled CLK A.





The Mod-2 Counter

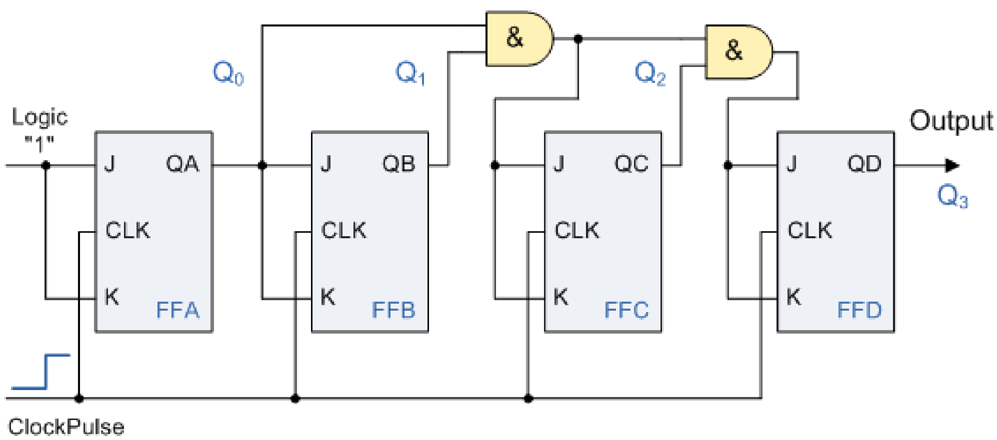
- Used by itself, Flip-flop A operates as a mod-2 counter.
- The count begins with a 0 at the Q output, and the maximum count occurs when the Q output is at a 1.
- The counter recycles back to 0 when the next clock pulse is applied.
- The mod-2 counter changes its count every time a negative edge of a clock pulse is applied to its clock input, which is labeled CLK A.



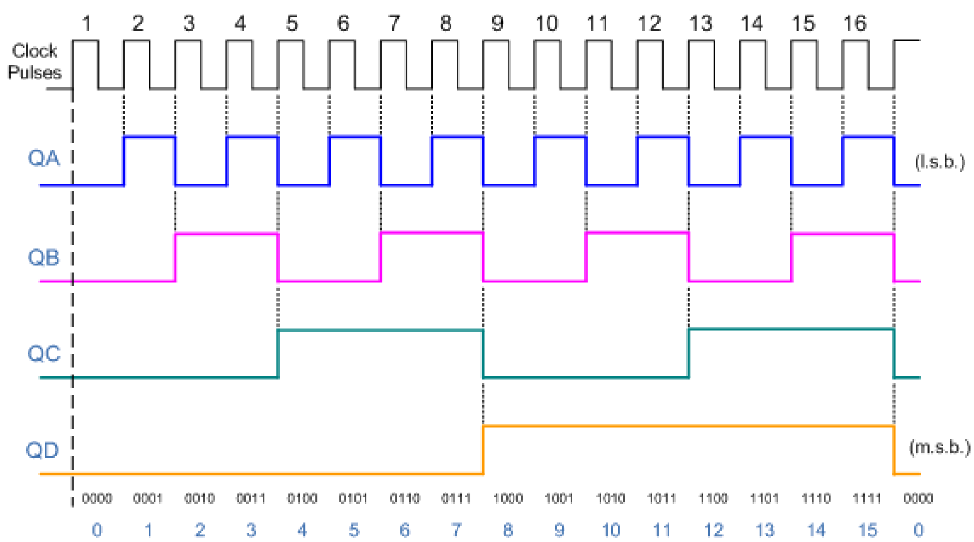
SYNCHRONOUS COUNTERS

In an asynchronous dual-port, read and write operations are triggered by a rising or falling signal. These can occur at any given time. In a synchronous dual-port, all read and write operations are synchronized to a clock signal. In other words, the operation begins at expected times.

Binary 4-bit Synchronous Counter



4-bit Synchronous Counter Waveform Timing Diagram

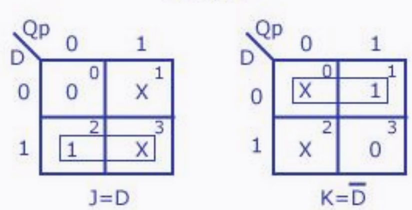


J-K Flip Flop to D Flip Flop

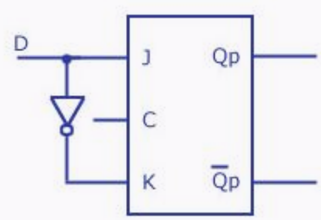
Conversion Table

D Input	Outputs Qp	Outputs Qp+1	J-K Inputs J	J-K Inputs K
0	0	0	0	X
0	1	0	X	1
1	0	1	1	X
1	1	0	X	0

K-maps

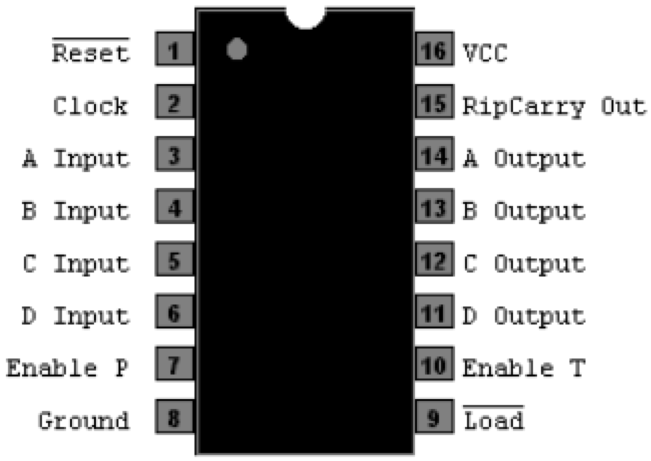


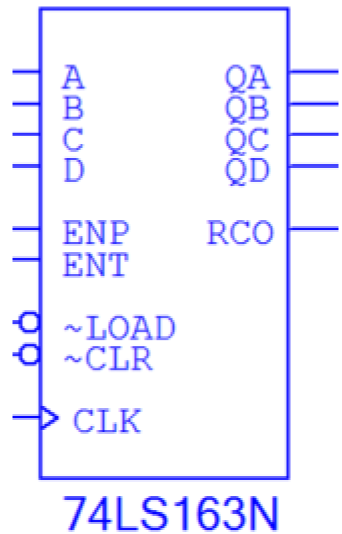
Logic Diagram



74LS163 4-Bit Synchronous UP counter

74LS163





74HC163 Medium Scale Integrated Circuit

• a 4 Bit Binary Counter packaged in 16 pin DIP (Dual In Line Package).

• IC is capable of counting from (0000) – (FFFF).

• the counter can be "synchronously" preset to any 4-bit binary number by applying the proper levels to the parallel data inputs.

• the number of input clock pulses will synchronously preset the 4-bit binary data into the counter.

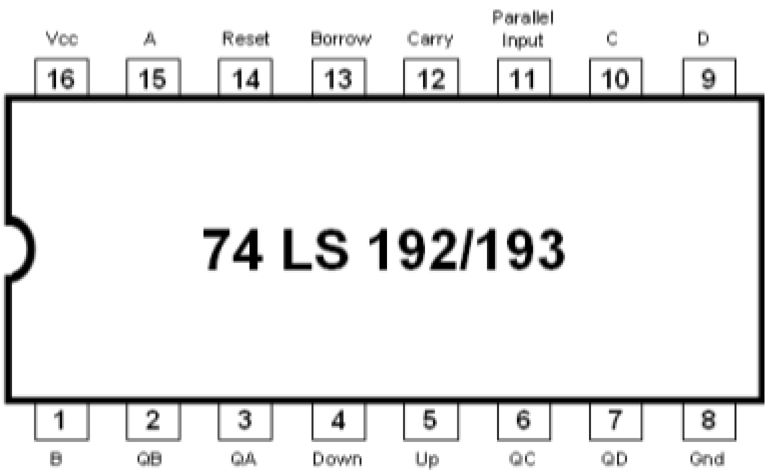
A,**B**,**C**,**D**	parallel data inputs; (A-LSB and D-MSB)
Q_A,**Q_B**,**Q_C**,**Q_D**	parallel outputs; (Q_A-LSB and Q_D-MSB)
RCO	is ripple carry output, this output is normally low and is asserted high when the device reaches it's maximum count.
ENT and **ENP**	are used for enabling the counter. Both ENT and ENP must be active (high) for the device to count.

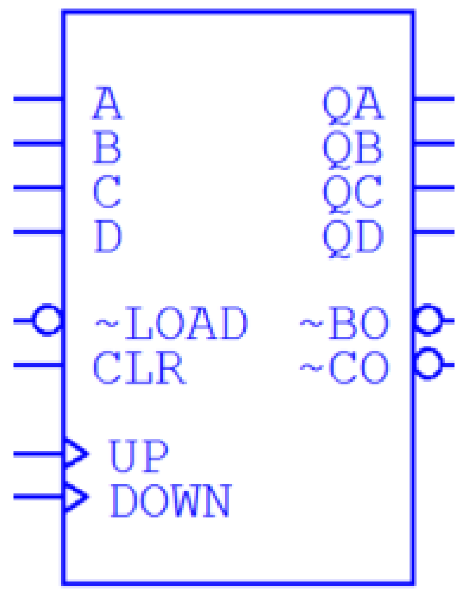
However, the ENT is also used in the production of RCO. Why is this?
One application is in the cascading of counters, covered later.

CLEAR	clears the counter.
LOAD	when active (low), the logic levels appearing at A - D are propagated to the outputs Q_A - Q_D.
CLK	is positive edge sensitive.

74LS193 4-Bit Synchronous UP/DOWN counter

74LS193





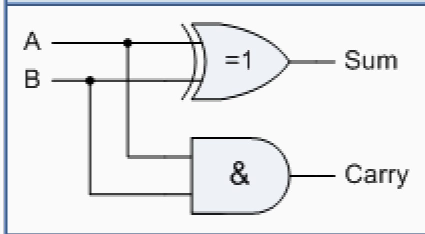
74LS193N

A,B,C,D	parallel data inputs; (A-LSB and D-MSB)
Q_A,Q_B,Q_C,Q_D	parallel outputs; (Q_A-LSB and Q_D-MSB)
CLEAR	clears the counter.
LOAD	when active (low), the logic levels appearing at A - D are propagated to the outputs Q_A - Q_D.
CLK	is positive edge sensitive.
UP	Up Counter Clock Input
DOWN	Down Counter Clock Input
~LOAD	Data Load
CLR	Clears The Counter
~BO	Borrow Output
~CO	Carry Output

Adders

1-Bit Half Adder

Symbol



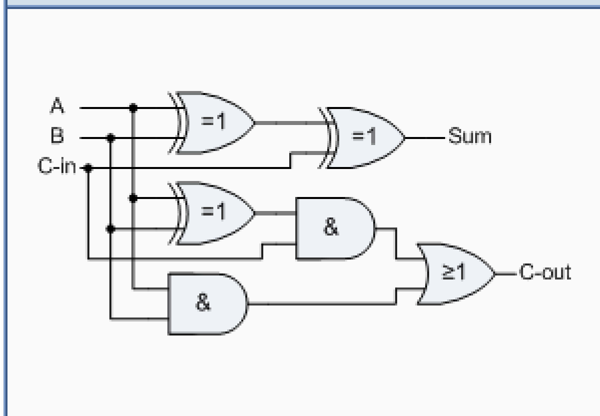
Truth Table

A	B	SUM	CARRY
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Boolean Expression: Sum = $A \oplus B$ Carry = $A . B$

Full Adder

Symbol

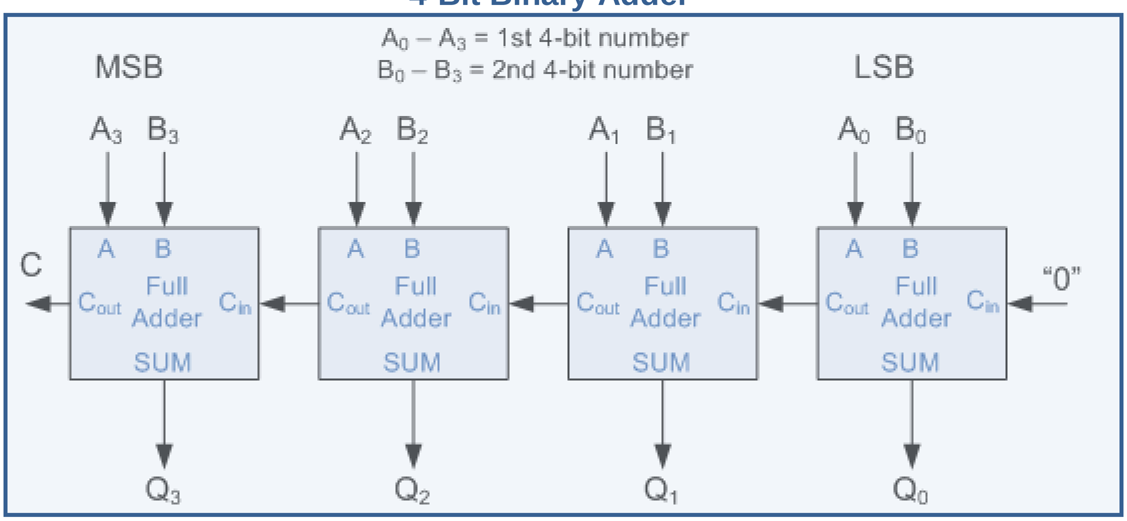


Truth Table

A	B	C-in	Sum	C-out
0	0	0	0	0
0	1	0	1	0
1	0	0	1	0
1	1	0	0	1
0	0	1	1	0
0	1	1	0	1
1	0	1	0	1
1	1	1	1	1

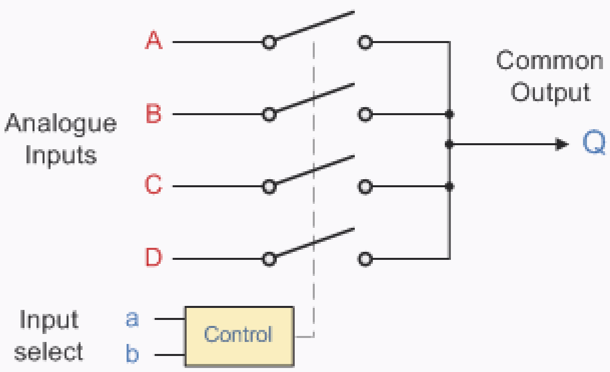
Boolean Expression: Sum = $A \oplus B \oplus C\text{-in}$

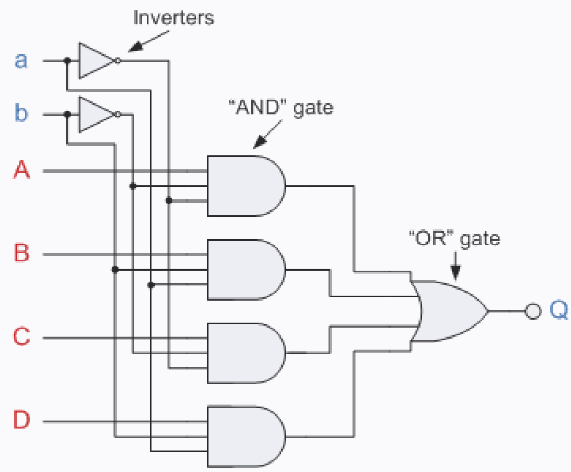
4-Bit Binary Adder



Multiplexer & De-Multiplexer

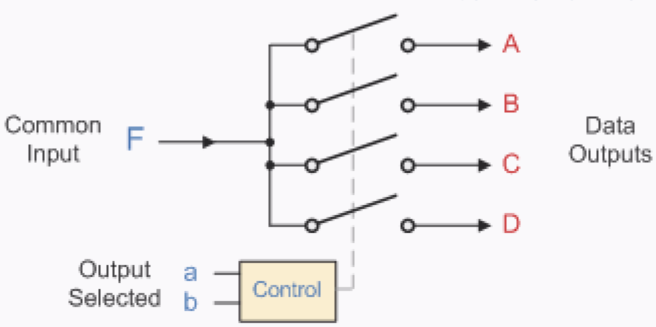
4-to-1 Channel Multiplexer (Mux)

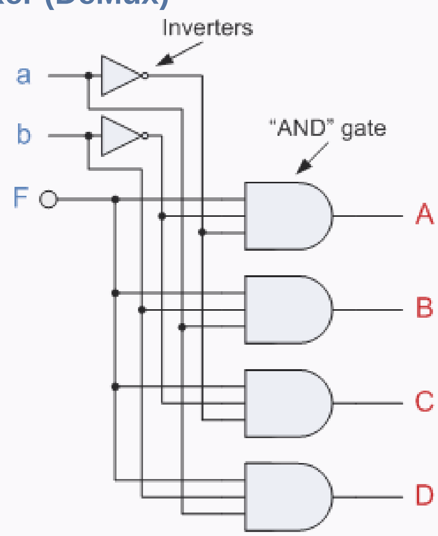




Addressing		Input Selected
b	a	
0	0	A
0	1	B
1	0	C
1	1	D

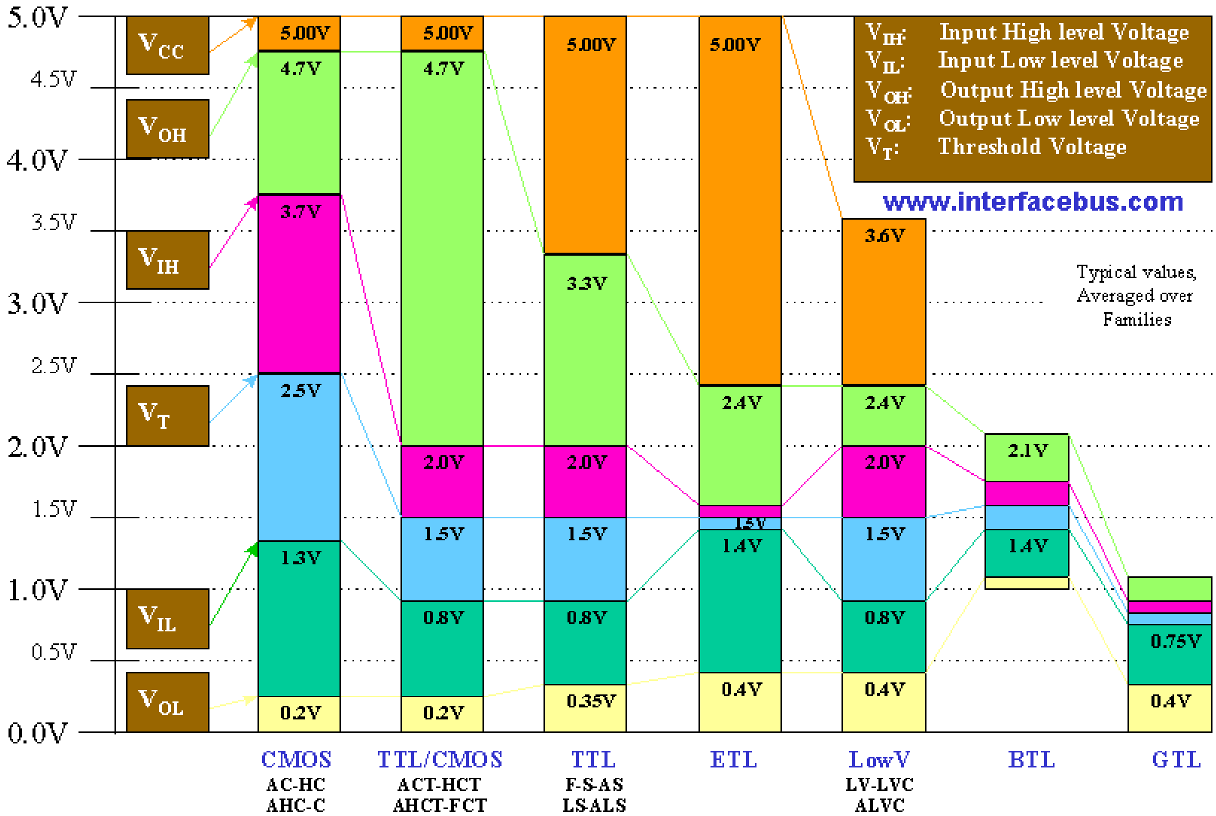
1-to-4 Channel De-Multiplexer (DeMux)





Addressing		Output Selected
b	a	
0	0	A
0	1	B
1	0	C
1	1	D

LOGIC VOLTAGE LEVELS



L298N Dual Full Bridge Driver