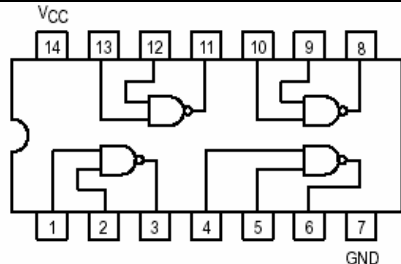
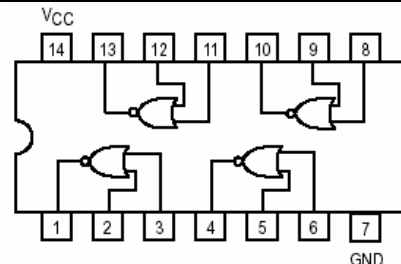
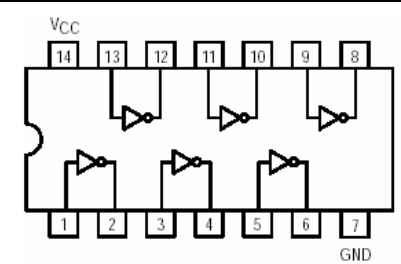
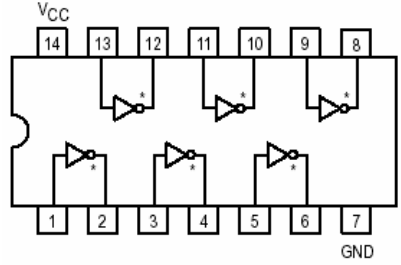
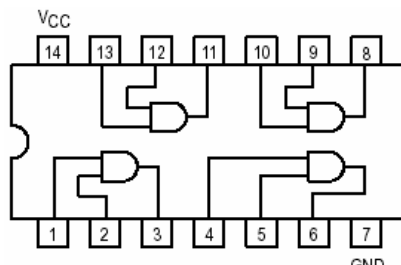
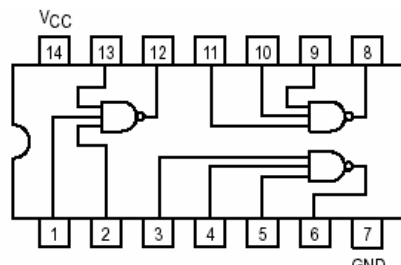
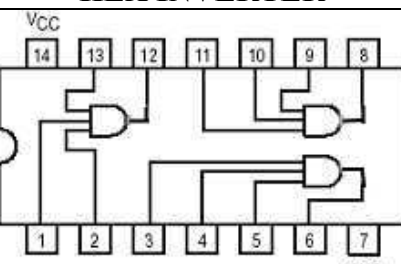
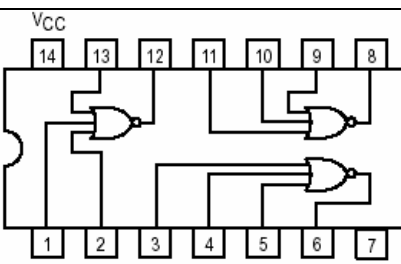
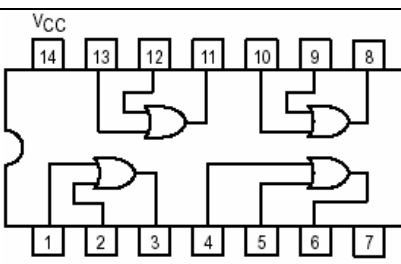
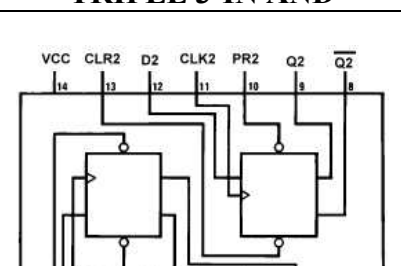
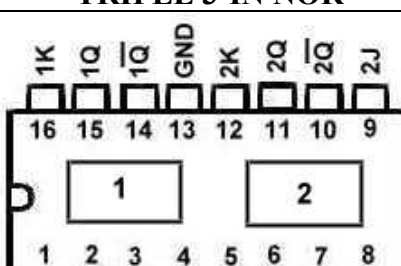
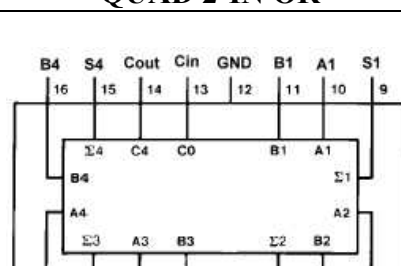
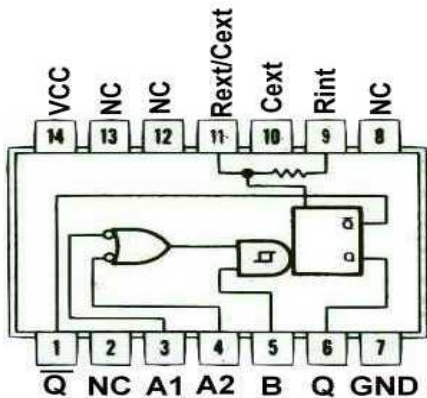


## INTEGRATED CIRCUIT PIN LAYOUT

 <p><b>74LS00</b> <b>QUAD 2-IN NAND</b></p>	 <p><b>74LS02</b> <b>QUAD 2-IN NOR</b></p>	 <p><b>74LS04</b> <b>HEX INVERTER</b></p>
 <p>* OPEN COLLECTOR OUTPUTS <b>74LS05</b> <b>HEX INVERTER</b></p>	 <p><b>74LS08</b> <b>QUAD 2-IN AND</b></p>	 <p><b>74LS10 &amp; 7410</b> <b>TRIPPLE 3-IN NAND</b></p>
 <p><b>74LS11</b> <b>TRIPLE 3-IN AND</b></p>	 <p><b>74LS27</b> <b>TRIPLE 3-IN NOR</b></p>	 <p><b>74LS32</b> <b>QUAD 2-IN OR</b></p>
 <p><b>74LS74</b> <b>DUAL D-FLIP FLOP</b></p>	 <p><b>74LS76</b> <b>DUAL J-K FLIP FLOP</b></p>	 <p><b>74LS83</b> <b>4-BIT FULL ADDER</b></p>

<p style="text-align: center;"><b>74LS86</b> <b>QUAD 2-IN EXOR</b></p>	<p style="text-align: center;"><b>74LS90</b> <b>DECADE COUNTER</b></p>	<p style="text-align: center;"><b>74LS93</b> <b>4-BIT COUNTER</b></p>
<p style="text-align: center;"><b>74LS121</b> <b>MONOSTABLE MULTI</b></p>	<p style="text-align: center;"><b>74LS125</b> <b>QUAD TRISTATE BUFFER</b></p>	<p style="text-align: center;"><b>74LS138</b> <b>3-to-8 DECODER/DEMUX</b></p>
<p style="text-align: center;"><b>74LS151</b> <b>1-of-8 SELECTOR/MUX</b></p>	<p style="text-align: center;"><b>74LS194</b> <b>4-BIT SHIFT REGISTER</b></p>	<p style="text-align: center;"><b>CD4016</b> <b>QUAD BILATERAL SWITCH</b></p>
<p style="text-align: center;"><b>CD4023</b> <b>TRIPPLE 3-IN NAND</b></p>		

### DETAILS OF THE 74LS121 MONOSTABLE MULTIVIBRATOR



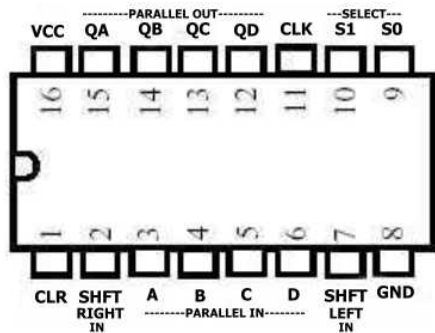
FUNCTION TABLE

INPUTS			OUTPUTS	
A1	A2	B	Q	$\bar{Q}$
L	X	H	L	H
X	L	H	L↑	H↑
X	X	L	L↑	H↑
H	H	X	L↑	H↑
H	L	H	□	□
L	H	H	□	□
L	L	H	□	□
L	X	↑	□	□
X	L	↑	□	□

Pulse Width,  $t_w = 0.7 * C_{ext} * R_{ext}$

**Ex:**  $C_{ext} = 0.001\mu f$ ,  $R_{ext} = 1K\Omega$ , will yield a Pulse Width,  $t_w = 70ns$

### DETAILS OF THE 74LS194 4-BIT SHIFT REGISTER



FUNCTION TABLE

CLEAR	MODE		CLOCK	SERIAL		PARALLEL				OUTPUTS			
	S1	S0		LEFT	RIGHT	A	B	C	D	QA	QB	QC	QD
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	QA0	QB0	QC0	QD0
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	QA <sub>n</sub>	QB <sub>n</sub>	QC <sub>n</sub>
H	L	H	↑	X	L	X	X	X	X	L	QA <sub>n</sub>	QB <sub>n</sub>	QC <sub>n</sub>
H	H	L	↑	H	X	X	X	X	X	QB <sub>n</sub>	QC <sub>n</sub>	QD <sub>n</sub>	H
H	H	L	↑	L	X	X	X	X	X	QB <sub>n</sub>	QC <sub>n</sub>	QD <sub>n</sub>	L
H	L	L	X	X	X	X	X	X	X	QA0	QB0	QC0	QD0

